496. (Amended) A voltage reference circuit responsive to an external voltage for supplying a reference voltage, comprising:

a constant current source for supplying a current to a node in response to the external voltage;

a circuit having an adjustable impedance for draining current from the node, wherein said circuit comprises a diode stack comprised of a plurality of transistors connected in series and a plurality of switches each switch for selectively shunting one of said transistors, and wherein each switch is responsive to a control signal; and

a unity gain amplifier responsive to a signal available at the node for producing the reference voltage.

499. (Amended) The voltage reference circuit of claim [498]496 wherein said switches are controlled by fuses[, and wherein opening certain of said fuses turns its associated switch on, and wherein opening certain other of said fuses turns its associated switch off].

Remarks

Claim 223 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Park (US Pat. No.: 5,448,199). Specifically, the Examiner states:

> Park discloses in figure 3 a voltage reference circuit responsive to an external voltage (ext. Vcc) for supplying a reference voltage (int. Vcc), comprising: an active reference circuit (10, 20, 30) for receiving the external voltage and for producing a reference signal (at node N2) having a desired relationship with the external voltage; and a unity gain amplifier (50) responsive to the reference signal for producing the reference voltage.

Claim 223 is amended to recite "said active reference circuit comprising a current source utilizing a current mirror for providing current to a diode stack having an adjustable impedance." It is respectfully submitted that Park does not disclose a current source utilizing a current mirror and does not disclose a diode stack having an adjustable impedance for removing current from the node. Thus, it is believed that claim 223 is in condition for allowance.

Claims 224, 496, and 497 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Park in view of Shibayama et al. (US Pat. No.: 5,554,953). Specifically, the Examiner stated:

> Park's figure 3 shows the active reference circuit comprises a current source (56). Park's figure 3 fails to show a diode stack having an adjustable

> impedance. However, Shibayama et al.'s figure 2 shows a method of replacing diode Qp6 of figure 1 with a diode stack (Qp16 of figure 2) having adjustable impedance for the purpose of capable adjusting the output reference voltage. Thus, it would have been obvious to one having ordinary skill in the art to replace Park's diode 58 (or 57 or both of diode 57 and 58) with Shibayama et al.'s diode stack for the purpose of capable of adjusting the output voltage of the reference circuit.

Claims 224 and 497 are cancelled. Claim 496 is amended to recite that the circuit having an adjustable impedance for draining current from the node includes a diode stack comprised of a plurality of series connected transistors and a plurality of switches for selectively shunting the transistors, and "wherein each switch is responsive to a control signal." It is respectfully submitted that Park in view of Shibayama does not disclose or suggest the use of diode stack comprised of a plurality of transistors with each controlled by a switch responsive to a control signal.

Park in view of Shibayama discloses a diode stack (Qp16) comprised of a group of p-type transistors. By connecting their gates to ground, each transistor remains in the "on" state. Each transistor has a fuse associated therewith. (See Fig. 3) The impedance of the transistor is added to the diode stack by opening its associated fuse . Thus, the ability to actively control the conductivity of the diode stack (Qp16) disclosed by Shibayama is limited.

The claimed invention, through the use of control signals connected to the gates of the transistor switches, provides more accurate control of the conductivity of the transistors in the diode stack. Thus, the claimed invention provides more accurate control of the diode stack's impedance. It is believed that claim 496 is in condition for allowance.

Claims 225 – 227 and 498 – 500 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Park in view of Shibayama et al. and Furumochi (US Pat. No.: 5,473,277). Claim 498 is cancelled. Claims 225 – 227 and claims 499 and 500 are dependent from allowable claims 223, and 496, respectively. Thus, it is believed that claims 225, 226, 227, 499, and 500 are in condition for allowance.

Claims 228 – 231 and 501 – 504 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Park. Claims 228 – 230 depend from allowable claim 223, and claims 501 – 503 depend from allowable claim 496. It is believed that claims 228 – 230 and claims 501 – 503 are in condition for allowance.

As to claims 231 and 504, the Examiner states:

> Park fails to teach a power amplifier stage for amplifying the reference voltage by a factor greater than unity to provide an output voltage. However, it is well know in the art that amplifier having the gain greater than unity is for providing an output having level greater that the level of input signal. Therefore, it would have been obvious to one having ordinary skill in the art to add a power amplifier having gain greater than unity to the output of Park's figure 3 for the purpose of providing an output signal greater than the int. Vcc level.

It is respectfully submitted that Park, Shibayama, and Furumochi do not teach or suggest amplifying the reference voltage by a factor greater than unity to provide an output voltage, and do not suggest using the series connection of a unity gain amplifier and a greater than unity gain amplifier. On the contrary, Park, Shibayama, and Furumochi disclose providing reference voltages that are less than an external voltage.

Park, for example, is directed to an internal voltage generation circuit with an adjustable burn-in voltage level. (Col. 1, lines 5 – 10.) The internal voltage generation circuit produces a reference voltage that is less than the external voltage. (Col. 1, lines 16 – 19.) Likewise, the burn-in voltage level produced is also less than the external voltage. (Col. 3, lines 56 – 65.) The voltages are maintained at a low level to reduce the electric field stress placed on the memory device's transistors. (Col. 1, lines 11 – 15.)

Shibayama, for example, is directed to an internal reduced voltage generator to be mounted in a semiconductor circuit. (Col. 1, lines 7 – 9.) Two reference voltages are produced, V_{ref} and V_{refbi}, each of which are less than Vcc. (Col. 4, lines 10 – 44.) As disclosed, V_{ref} is used for normal operation and V_{refbi} is used for burn-in acceleration tests. (Col. 3, lines 22 – 25.)

Furumochi, for example, is directed to a constant voltage generator circuit. (Col. 5, lines 18 – 39.) More specifically, Furumochi is directed to a constant voltage generator circuit with a transistor back-gate voltage adjustment means to provide a higher precision constant voltage V_{DD}. (Col. 5, line 55 to Col. 6, line 62.) By controlling the number of transistors connected between an external voltage Vss and ground, the constant voltage generator circuit disclosed in Furumochi produces an output voltage that is less than an external voltage. (Col. 5, line 55 to Col. 6, line 62.)

As illustrated in the discussion above, Park, Shibayama et al., and Furumochi do not disclose or suggest adding a power amplifier having gain greater than unity in series with a unity gain amplifier responsive to the output of an active reference circuit for the purpose of providing an output signal greater than the internal Vcc level. On the contrary, Park, Shibayama et al., and Furumochi are directed to generating an internal voltage level which is less than an external voltage level. It is believed that claims 231 and 504 are in condition for allowance, and thus, it is respectfully requested that the rejection of claims 231 and 504 be withdrawn.

Claims 232 – 237, 247 and 505 – 510 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Hayakawa (US Pat. No.: 5,184,031) in view of Park. Specifically, the Examiner states:

> Hayakawa shows in figure 1 a circuit for supplying the external voltage as the output voltage when the external voltage is below a first predetermined value and supplying a step down voltage when the external voltage is above the

predetermined value. Thus, Hayakawa shows all limitations of the claim except for the detail of the internal stepdown circuit (13). However, Park's figure 3 shows a detail of an internal step down circuit (see the rejection of claim 231). Park's figure 3 having an advantage of providing a stable internal signal. Therefore, it would have been obvious to one having ordinary skill in the art to use Park's internal circuit for Hayakawa et al's internal stepdown circuit (13) for the purpose of providing a stable signal.

It is respectfully submitted that claims 232 – 237 and 505 – 510 are dependant from allowable claims 231 and 504, respectively. Hayakawa (as is the case with Park, Shibayama, and Furumochi) fails to disclose or suggest adding a power amplifier having gain greater than unity in series with a unity gain amplifier responsive to the output of an active reference circuit for the purpose of providing an output signal greater than the internal Vcc level. Thus, Hayakawa does not "show all the limitations of the claims[s]." It is believed that claims 232 – 237 and 505 – 510 are in condition for allowance and it is respectfully requested that the rejection of claims 232 – 237 and 505 – 510 be withdrawn.

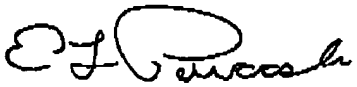
With respect to claim 247, the Examiner states that "claim 247 recites similar limitations of claims 232 – 237, therefore, it is rejected for the same reasons." It is respectfully submitted that Park, Shibayama, Furumochi, and Hayakawa fail to disclose or suggest "amplifying the reference signal with a unity gain amplifier" and "amplifying the reference voltage by a factor greater than unity to provide the output voltage when the external voltage is not being supplied as the output voltage" as recited in claim 247. It is believed that claim 247 is in condition for allowance. Thus, it is respectfully requested that the rejection of claim 247 be withdrawn.

Claims 248 – 250 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Hayakawa in view of Park and Shibayama. Claims 248 – 250 depend from allowable base claim 247 and are believed to be in condition for allowance for the same reasons as discussed in conjunction with base claim 247. Thus, it is respectfully requested that the rejection of claims 248 – 250 be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. Accordingly, a Notice of Allowance for claims 223, 225 – 237, 247 – 250, 496, and 499 – 510 is respectfully requested. If the Examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the Examiner is respectfully requested to contact applicants' attorney at the telephone number listed below so that additional changes may be discussed.

A complete set of the claims currently pending is enclosed herewith.

Respectfully submitted



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